BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

ECE-322
Electronic Circuits (B)

Lecture #8
Phase-locked Loop (PLL)

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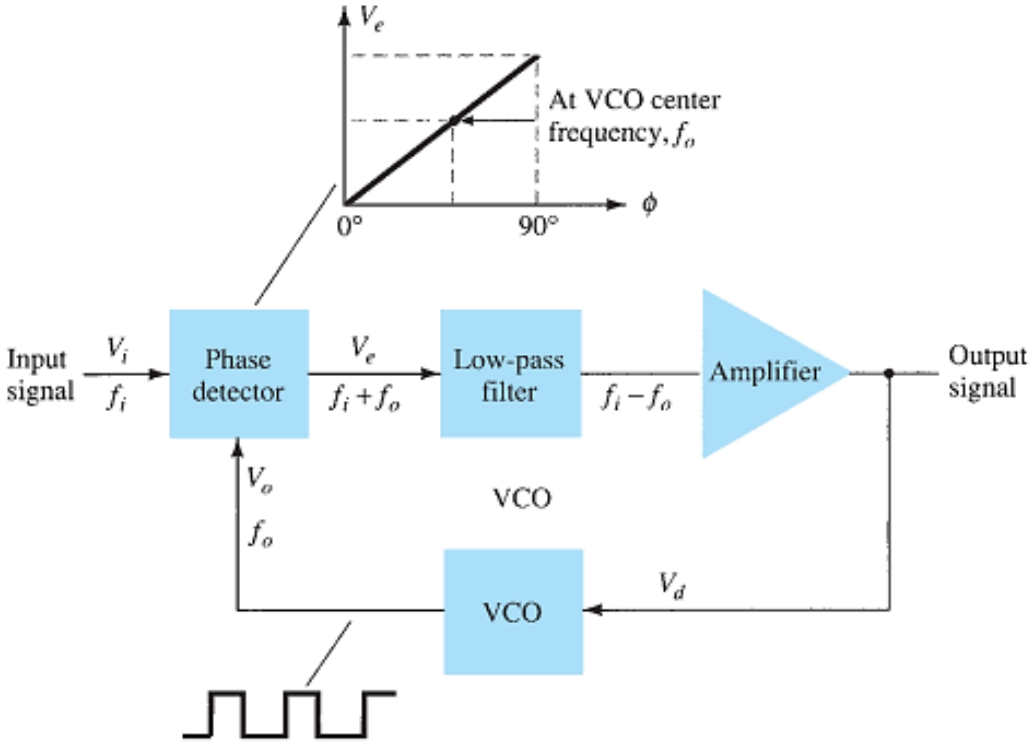
Agenda

- Introduction
- Basic Operation
- Applications

Intro.

- A phase-locked loop (PLL) is an electronic circuit that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator connected as shown.



- The closed-loop operation of the circuit is to **maintain** the **VCO frequency locked to** that of the **input** signal **frequency**.

Intro..

- Common applications of a PLL include:
  - **Frequency synthesizers** that provide multiples of a reference signal frequency.
  - **FM demodulation networks** for FM operation with excellent linearity between the input signal frequency and the PLL output voltage.
  - **Demodulation of** the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (**FSK**) operation.
  - wide variety of areas including **modems**, **telemetry receivers** and **transmitters**, **tone decoders**, **AM detectors**, and **tracking filters**.

Basic Operation..

- Capture and Lock operation:
  - Within a capture-and-lock frequency range, the **dc voltage** will **drive** the **VCO frequency** to **match** that of the **input**.
  - While the loop is trying to achieve lock, the **output** of the phase comparator **contains frequency components at the sum and difference** of the signals compared.
  - A **low-pass filter passes** only the **lower frequency** component of the signal, so that the loop can obtain lock between input and VCO signals.

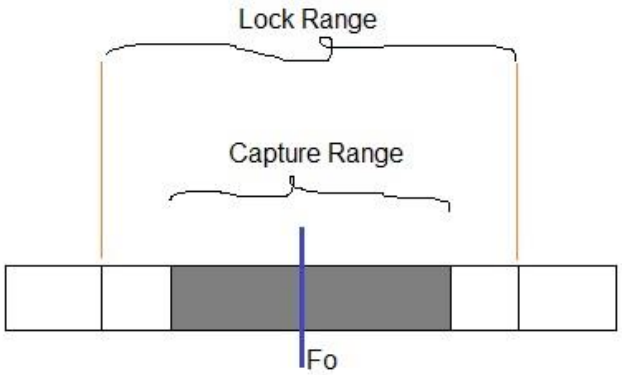
Basic Operation

- lock operation:
  - **input** signal frequency is the **same as** that from the **VCO** .
  - **Best operation** is **obtained** if the **VCO center frequency** $\mathbf{f_o}$ is set with the dc bias voltage **midway** in its **linear** operating range.
  - The **amplifier** allows this **adjustment** in **dc voltage** from that obtained as output of the filter circuit.
  - **When** the **loop** is in **lock**, the **two signals** to the comparator are of the **same frequency**, although **not necessarily** in **phase**.
  - A **fixed phase** difference between the two signals to the comparator results in a **fixed dc voltage** to the VCO.
  - **Changes in** the **input** signal frequency then result in change in the dc voltage to the VCO.

Basic Operation…

- Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are **two** important **frequency bands** specified for a PLL.

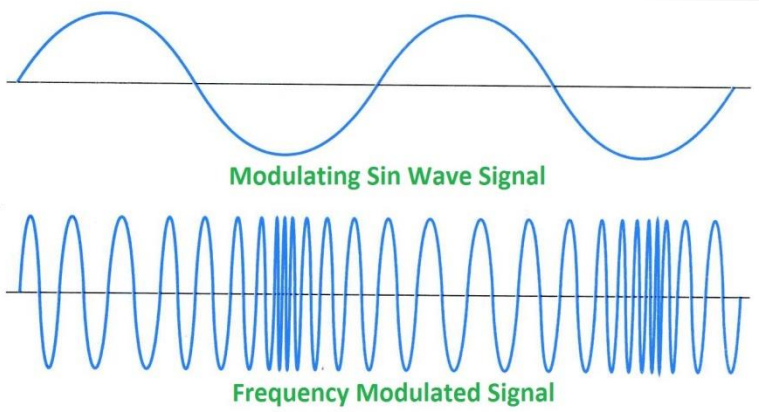
- The **capture** range of a PLL is the frequency range centered about the VCO free-running frequency f_o over which the loop can acquire lock with the input signal.
- Once the PLL has achieved capture, it can maintain **lock** with the input signal over a somewhat wider frequency range called the lock range.

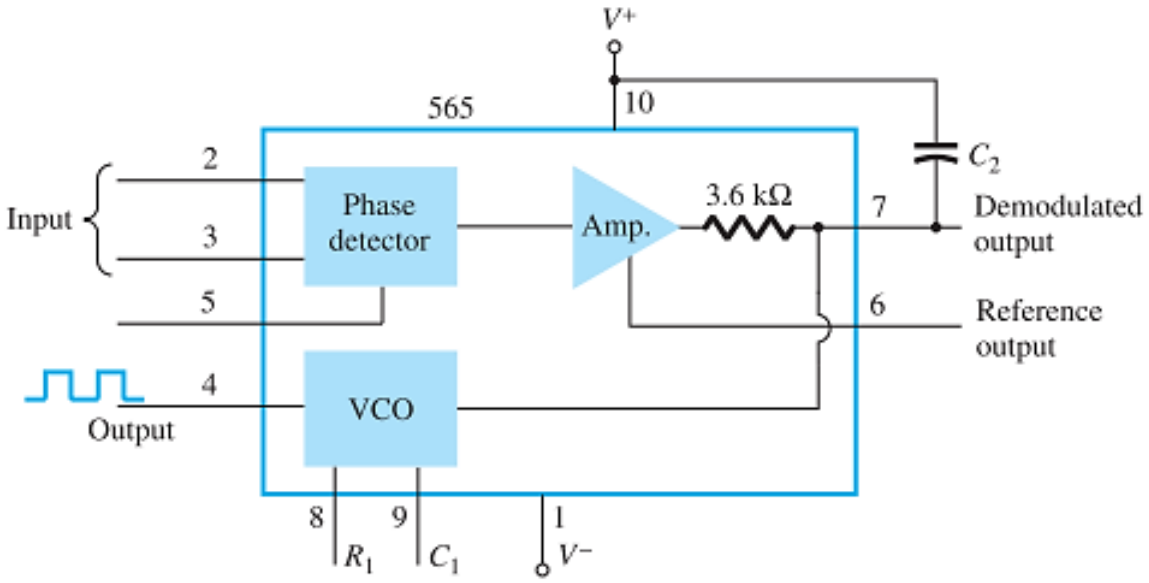


Fo = VCO Free Running Frequency

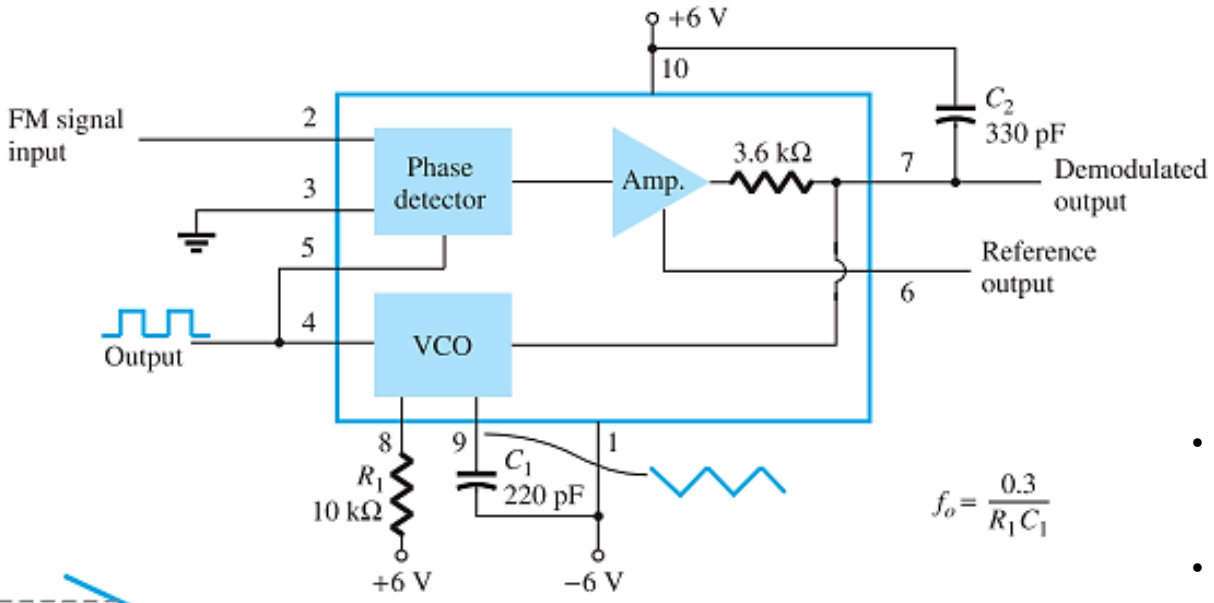
Applications
Frequency Demodulation

- The PLL center frequency is selected or designed at the FM carrier frequency.
- The filtered or output voltage is the desired demodulated voltage, varying in value in proportion to the variation of the signal frequency.



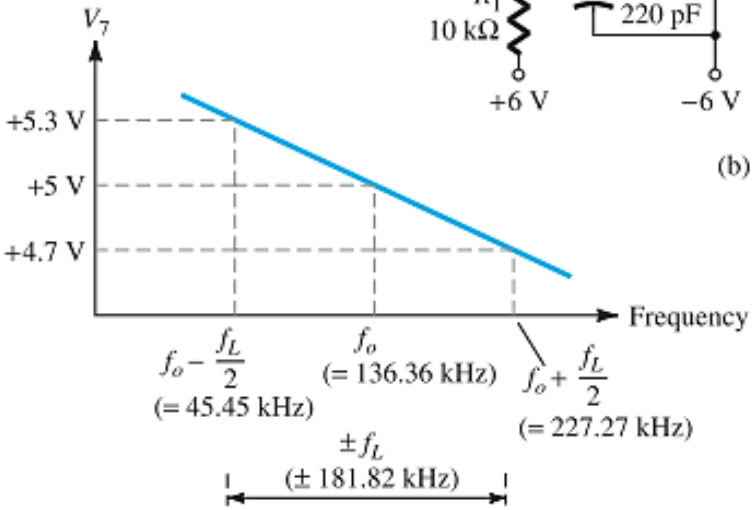


Applications
Frequency Demodulation..



$$f_o = \frac{0.3}{R_1 C_1}$$

- R_1&C_1 → set the center frequency of the VCO.
- C2 → sets the LPF passband



(b)

- Lock range:

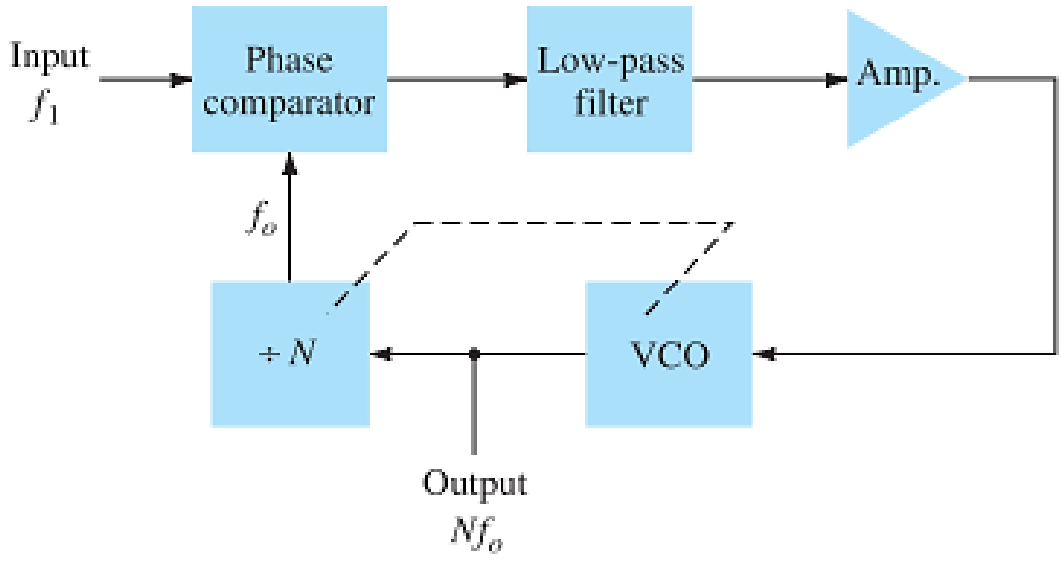
$$f_L = \pm \frac{8 f_o}{V}$$

- Capture range:

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{R_2 C_2}}$$

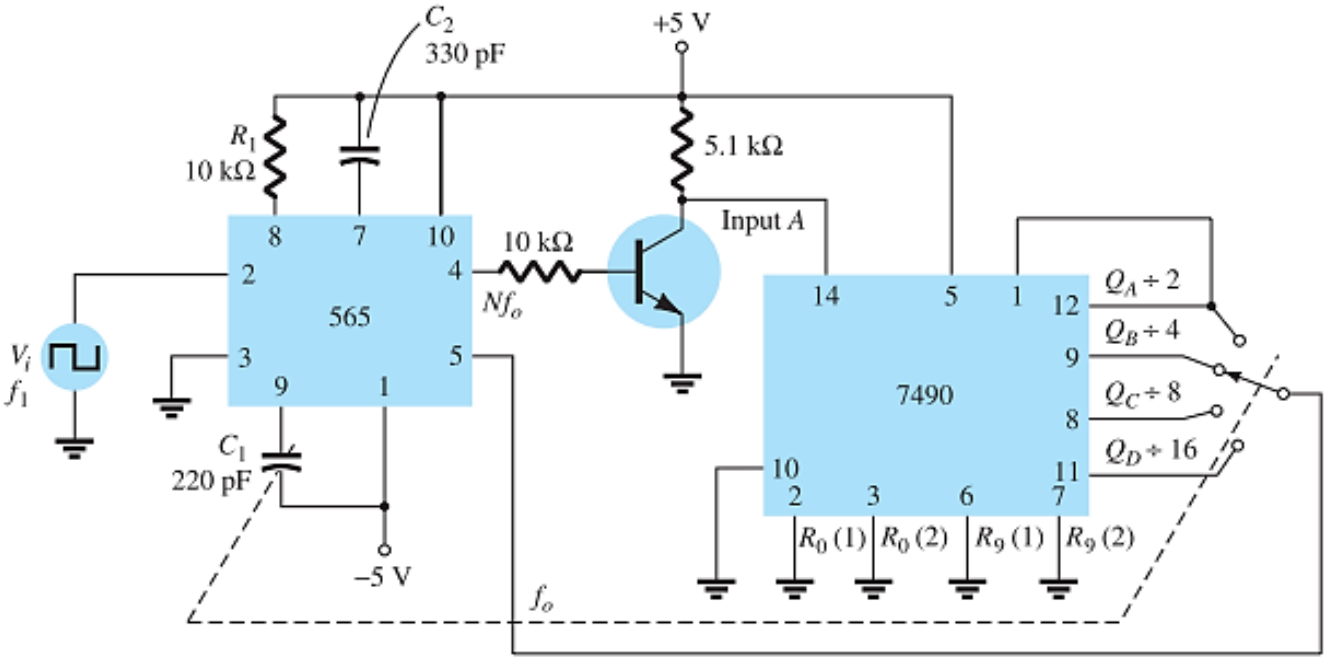
Applications
Frequency Synthesis

- A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o and the VCO output is Nf_o.
- This output is a multiple of the input frequency as long as the loop is in lock.



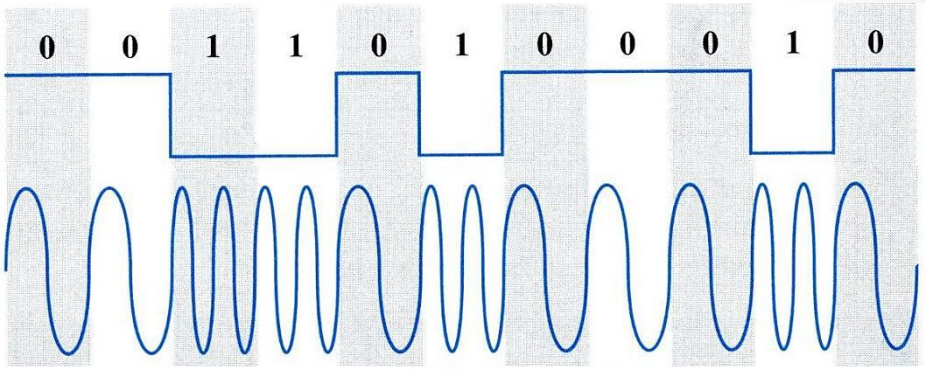
Applications
Frequency Synthesis..

- example using a 565 PLL as frequency multiplier and a 7490 as divider.



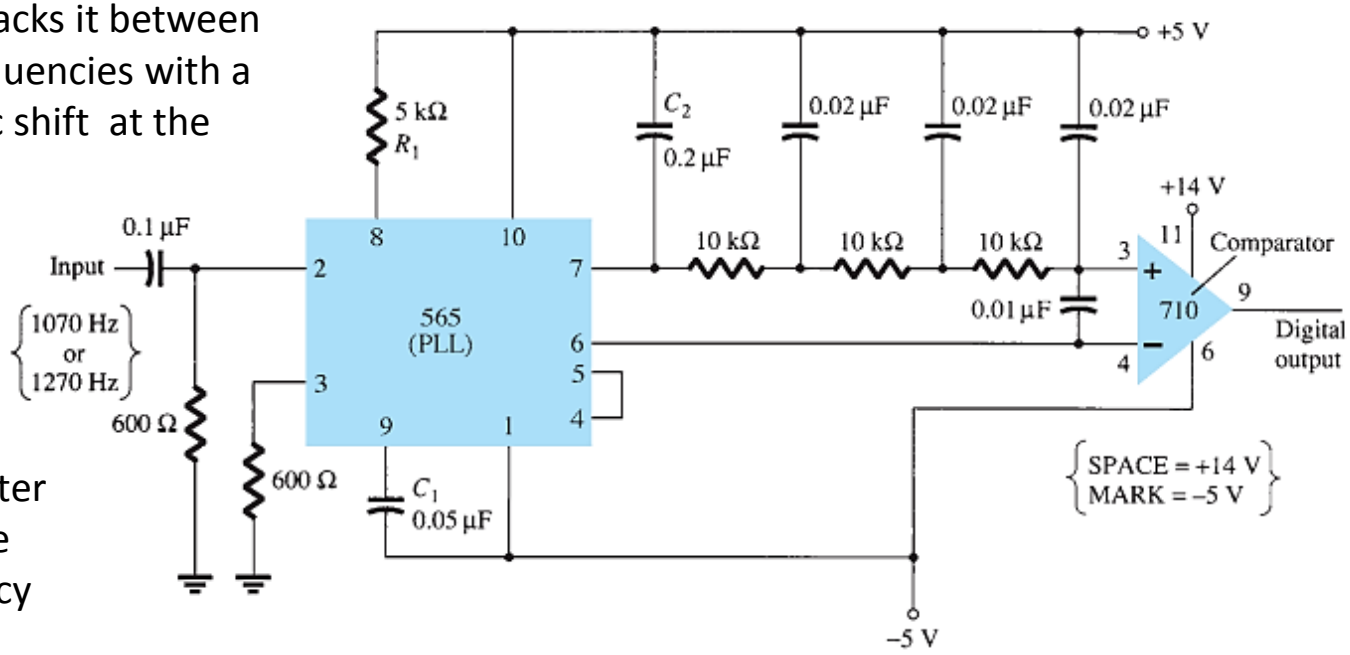
Applications
FSK Decoders

- The decoder receives a signal at one of two distinct carrier frequencies, 1270 Hz or 1070 Hz, representing the RS-232C logic levels or mark (-5 V) or space (+14 V), respectively.
- As the signal appears at the input, the loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output.



Frequency Shift Keying (FSK)

Two frequencies to represent 0 & 1



- The RC ladder filter is used to remove the sum-frequency component.

Now, let's go to CAD ☺

- For more details, refer to:
  - Chapter 13, Boylestad, **Electronic Devices and Circuits**, 11th edition.
- The lecture is available online at:
  - http://bu.edu.eg/staff/ahmad.elbanna-courses/12135
- For inquires, send to:
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